

MULTIMEDIA



UNIVERSITY

STUDENT ID NO

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MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2018/2019

EEE4186 - VLSI SYSTEM DESIGN AND MODELING TECHNIQUE (EE)

14 MARCH 2019
2:30 PM – 4:30 PM
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of **6 pages** including cover page with **4 Questions** only.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is the same.
3. Please print all your answers in the answer Booklet provided.
4. A **VHDL model** means an entity-architecture pair, plus any extra codes that might be necessary for them to work properly (library, use, etc.)
5. When names (of entities, architectures, signals, etc.) are not specified, you may use any suitable and valid name.

Question 1

- (a) Construct the *entity* of the full adder (Figure Q1) in VHDL. Use entity name: *full_adder*.

[6 marks]

- (b) Design the *architecture* of the full adder (Figure Q1) by modelling the characteristic equation of the output signals, S and C_{out} in VHDL. Use architecture name: *full_adder_arch*.

[6 marks]

- (c) Write the *architecture* of the full adder (Figure Q1) using **structural** VHDL code by instantiate *component* *xor2*, *and2* and *or2*. Use architecture name: *full_adder_arch*, and the signal *sig1*, *sig2* and *sig3* shown in Figure Q1.

[13 marks]

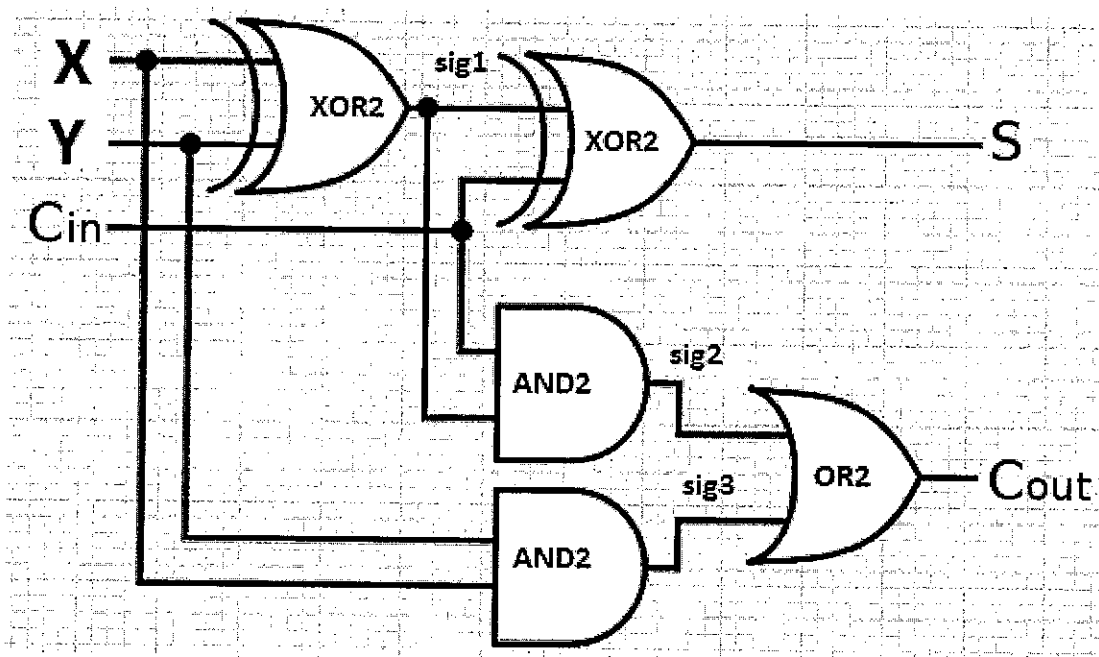


Figure Q1

Continued ...

Question 2

- (a) Create the entity of the 8-to-1 multiplexer (Figure Q2) in VHDL. Use entity name: *mux8*.

[5 marks]

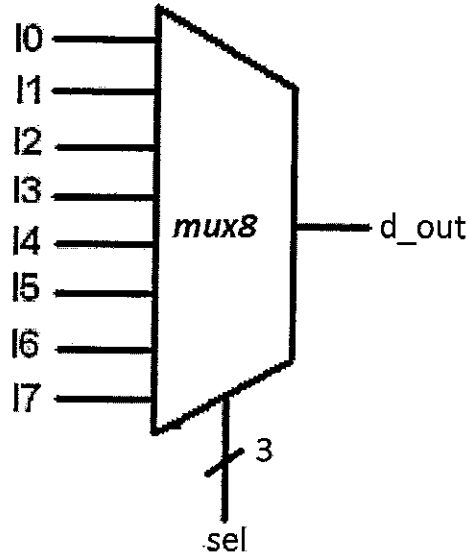


Figure Q2

- (b) Design the *architecture* of the 8-to-1 multiplexer (Figure Q2) in VHDL using the following styles. Use architecture name: *mux8_arch*.
- (i) Selected signal assignment
 - (ii) Conditional signal assignment
 - (iii) IF construct

[7+6+7 marks]

Continued ...

Question 3

- (a) Synthesize the VHDL code shown in Figure Q3 by using the logic gates.

[4 marks]

```
entity half_adder IS
port ( A,B      : in bit;
      CARRY,SUM : out bit);
end half_adder;

architecture arch of half_adder is
begin
  ADD: process (A,B)
  begin
    SUM <= A xor B;
    CARRY <= A and B;
  end process ADD;
end arch;
```

Figure Q3

- (b) Create a test-bench in VHDL code to test the circuit in part (a), by referring to the *work.half_adder(arch)*. The time step for the test-bench is 100ns.

[12 marks]

- (c) Create the truth table of the circuit in part (a).

[4 marks]

- (d) Sketch a waveform diagram to represent the test-bench signal(s) that you created in part (b), and include the expected output in your waveform.

[5 marks]

Continued ...

Question 4

- (a) Synthesize the VHDL code shown in Figure Q4a using the logic gates, multiplexer and D flip-flop.

[6 marks]

```

library ieee;
use ieee.std_logic_1164.all;

entity circuitq4 is
port (clk, t: in std_logic;
      q: out std_logic);
end circuitq4;

architecture arch of circuitq4 is
  signal tq : std_logic;
begin
  process (clk)
  begin
    if clk = '1' then
      if t = '1' then
        tq <= not tq;
      end if;
    end if;
  end process;
  q <= tq;
end arch;

```

Figure Q4a

- (b) Sketch the finite state machine diagram of the VHDL code shown in Figure Q4b. State the type of the finite state machine shown in Figure Q4b.

[8 marks]

<pre> entity q4b is port (clk, rst, a: in bit; b: out bit); end q4b; architecture arch of q4b is type state_type is (X, Y); signal current_state: state_type; begin process (clk, rst) begin if rst = '1' then current_state <= X; elsif clk'event and clk = '1' then case current_state is when X => if a = '0' then current_state <= X; else current_state <= Y; </pre>	<pre> when Y => if a = '1' then current_state <= Y; else current_state <= X; end case; end if; end process; process (current_state, a) begin case current_state is when X => b <= '0'; when Y => b <= a; end case; end process; end arch; </pre>
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Figure Q4b

Continued ...

- (c) Draw the state table of the finite state machine shown in Figure Q4b. [6 marks]
- (d) Sketch the output waveform, b, corresponding to the input signals shown in Figure Q4d. [5 marks]

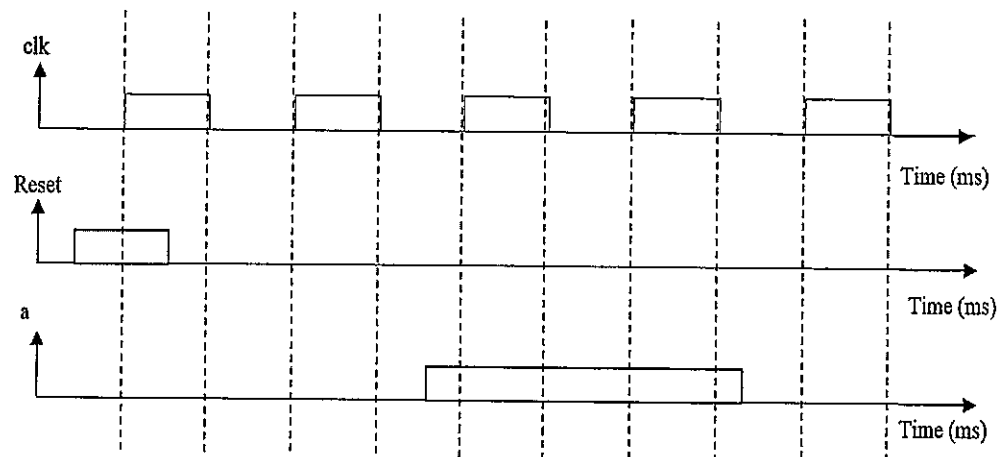


Figure Q4d

End of Paper